SI65R580FS2

650V 0.60Ω N-channel MOSFET

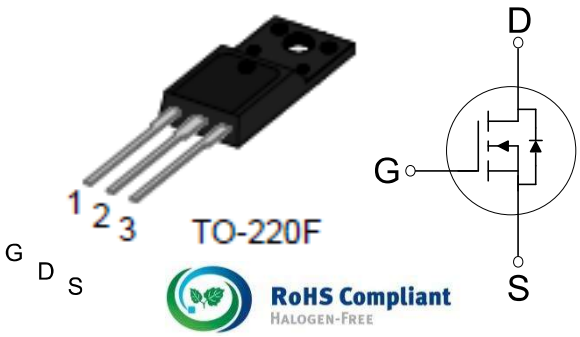
■ Description

SI65R580FS2 is power MOSFET using Magnachip's advanced super junction technology that can realize very low on-resistance and gate charge. It will provide much high efficiency by using optimized charge coupling technology. These user friendly devices give an advantage of Low EMI to designers as well as low switching loss.

■ Key Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,\,max}$	700	V
$R_{DS(on),\,max}$	0.60	Ω
$V_{GS(th),\,typ}$	3	V
I_D	7.3	A
$Q_{g,\,typ}$	13.8	nC

■ Package & Internal Circuit



■ Features

- Low Power Loss by High Speed Switching and Low On-Resistance
- 100% Avalanche Tested
- Green Package – Pb Free Plating, Halogen Free

■ Applications

- PFC Power Supply Stages
- Switching Applications
- Adapter

■ Ordering Information

Order Code	Marking	Temp. Range	Package	Packing	RoHS Status
SI65R580FS2	SI65R580	-55 ~ 150℃	TO-220F	Tube	Compliant

■ Absolute Maximum Rating (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Rating	Unit	Note
Drain – Source voltage	V_{DSS}	650	V	
Gate – Source voltage	V_{GSS}	±30	V	
Continuous drain current	I_D	7.3	A	T_C=25°C
		4.6	A	T_C=100°C
Pulsed drain current(1)	I_{DM}	21.9	A	
Power dissipation	P_D	25	W	
Single - pulse avalanche energy	E_{AS}	142	mJ	
MOSFET dv/dt ruggedness	dv/dt	50	V/ns	
Diode dv/dt ruggedness(2)	dv/dt	15	V/ns	
Storage temperature	T_{stg}	-55 ~150	℃	
Maximum operating junction temperature	T_j	150	℃	

1) Pulse width t_P limited by $T_{j,max}$
2) $I_{SD} \leq I_D$, $V_{DS\ peak} \leq V_{(BR)DSS}$

■ Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case max	R_{thjc}	5	℃/W
Thermal resistance, junction-ambient max	R_{thja}	75	℃/W

■ Static Characteristics (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain – Source Breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS} = 0V, I_D = 250uA
Gate Threshold Voltage	$V_{GS(th)}$	2	3	4	V	V_{DS} = V_{GS}, I_D = 250uA
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	uA	V_{DS} = 650V, V_{GS} = 0V
Gate Leakage Current	I_{GSS}	-	-	100	nA	V_{GS} = ±30V, V_{DS} = 0V
Drain-Source On State Resistance	$R_{DS(ON)}$	-	0.54	0.60	Ω	V_{GS} = 10V, I_D = 2.1A

■ Dynamic Characteristics (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{iss}	-	545	-	pF	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	640	-		
Reverse Transfer Capacitance	C_{rss}	-	28.6	-		
Effective Output Capacitance Energy Related (3)	$C_{o(er)}$	-	18.8	-		V_{DS} = 0V to 520V, V_{GS} = 0V, f = 1.0MHz
Turn On Delay Time	$t_{d(on)}$	-	18	-	ns	V_{GS} = 10V, R_G = 25Ω, V_{DS} = 325V, I_D = 7.3A
Rise Time	t_r	-	33	-		
Turn Off Delay Time	$t_{d(off)}$	-	80	-		
Fall Time	t_f	-	28	-		
Total Gate Charge	Q_g	-	13.8	-	nC	V_{GS} = 10V, V_{DS} = 520V, I_D = 7.3A
Gate – Source Charge	Q_{gs}	-	3.6	-		
Gate – Drain Charge	Q_{gd}	-	5.6	-		
Gate Resistance	R_G	-	20	-	Ω	V_{GS} = 0V, f = 1.0MHz

3) $C_{o(er)}$ is a capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0V to 80% $V_{(BR)DSS}$

■ Reverse Diode Characteristics (T_c=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Continuous Diode Forward Current	I_{SD}	-	-	7.3	A	
Diode Forward Voltage	V_{SD}	-	-	1.4	V	I_{SD} = 7.3A, V_{GS} = 0V
Reverse Recovery Time	t_{rr}	-	272	-	ns	I_{SD} = 7.3A di/dt = 100A/μs V_{DD} = 100V
Reverse Recovery Charge	Q_{rr}	-	3	-	uC	
Reverse Recovery Current	I_{rrm}	-	22.2	-	A	

■ Characteristic Graph

Fig.1 On-Region Characteristics.

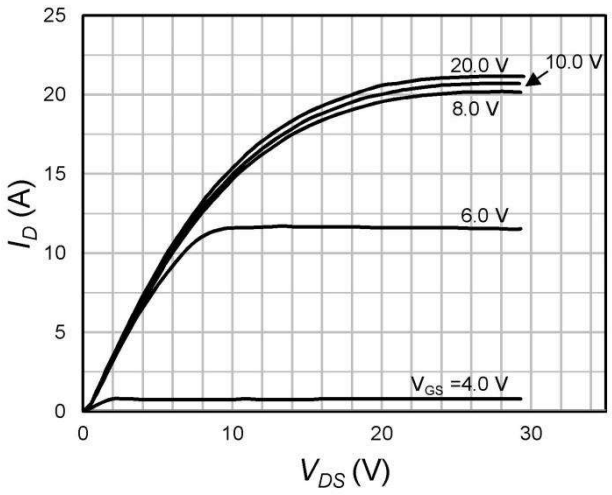


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

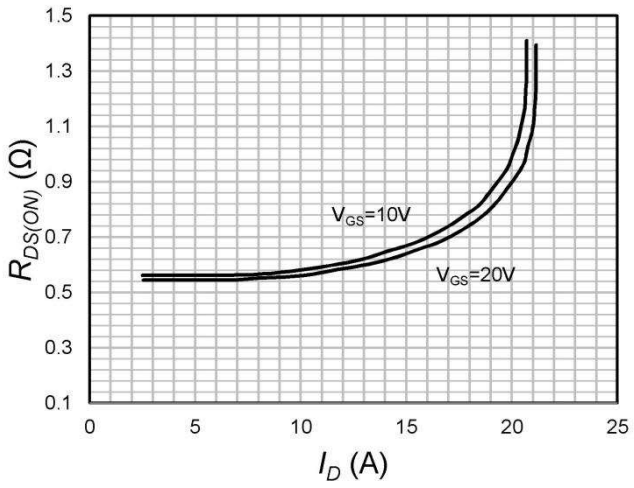


Fig.3 On-Resistance Variation with Temprature (Normalized)

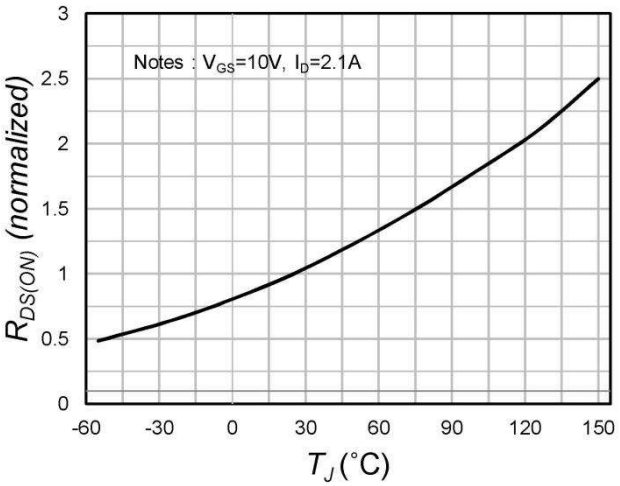


Fig.4 Breakdown Voltage Variation vs. Temperature (Normalized)

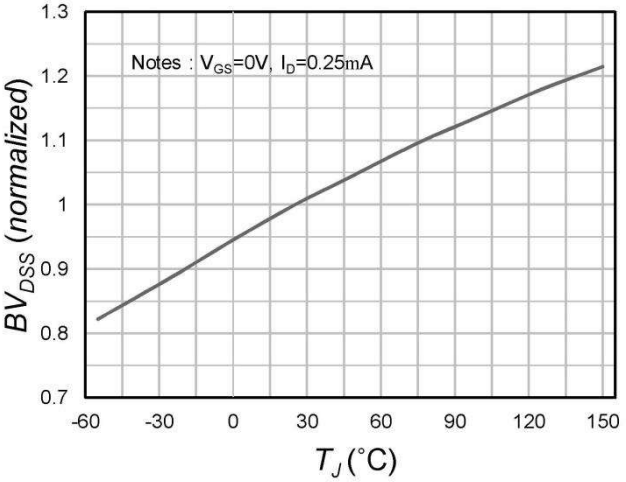


Fig.5 Transfer Characteristics

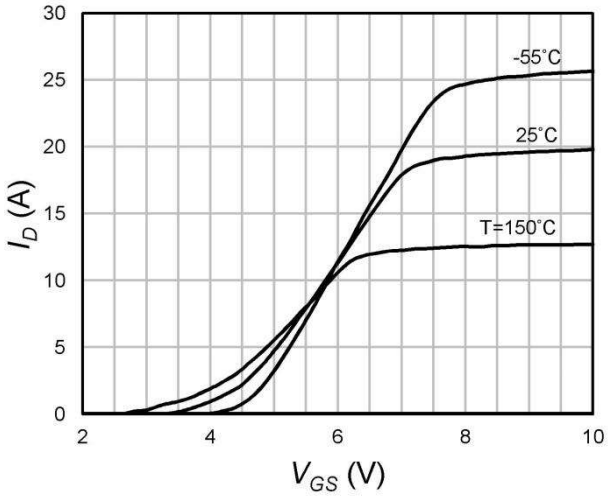


Fig.6 Body Diode Forward Voltage Variation with Source Current and Temperature

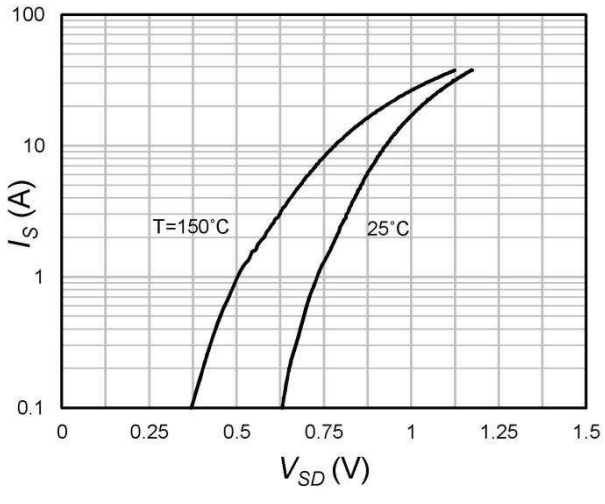


Fig.7 Gate Charge Characteristics

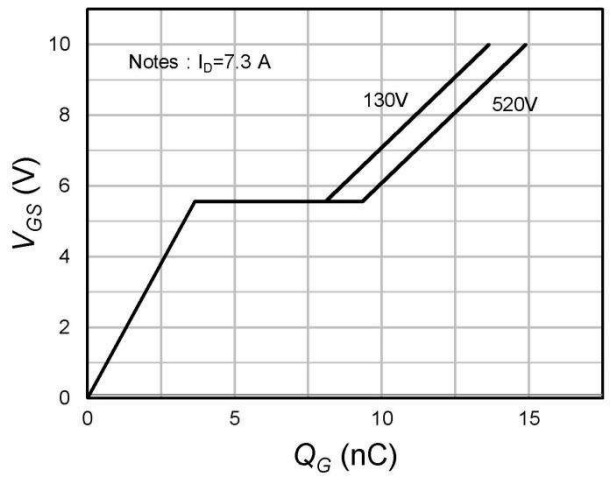


Fig.8 Capacitance Characteristics

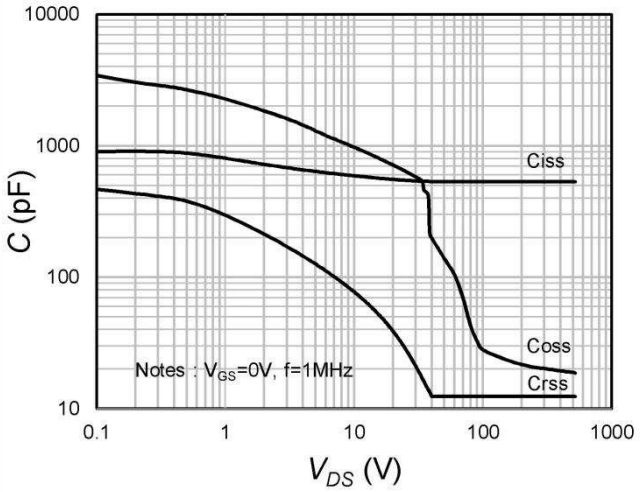


Fig.9 $V_{GS(th)}$ Variation with Temprature (Nomalized)

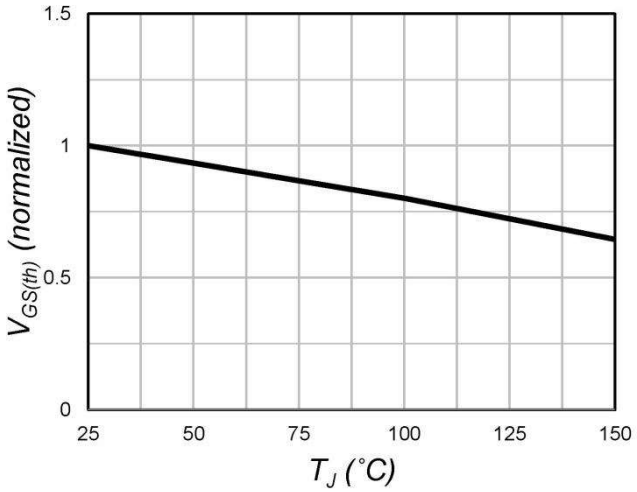


Fig.10 Maximum Drain Current vs. Case Temperature

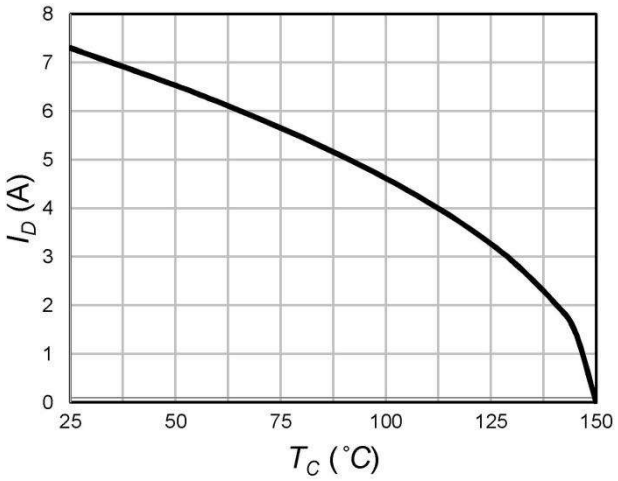


Fig.11 Single Pulse Maximum Power Dissipation

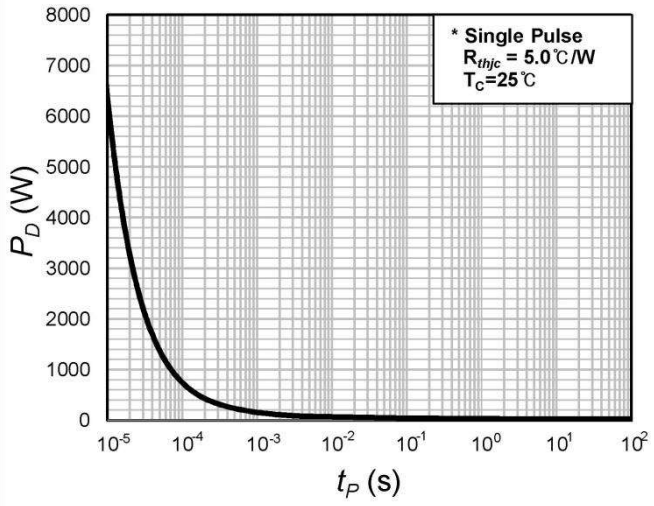


Fig.12 Output Capacitance Stored Energy

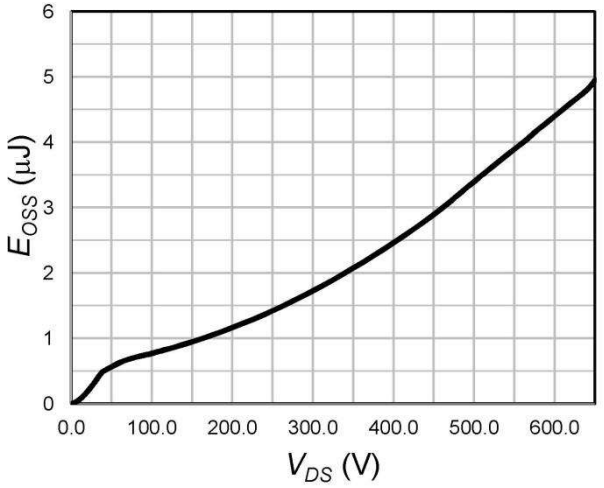


Fig.13 Transient Thermal Response Curve

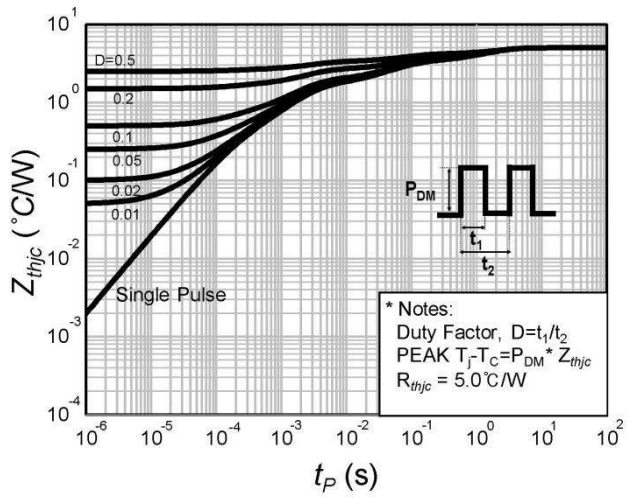
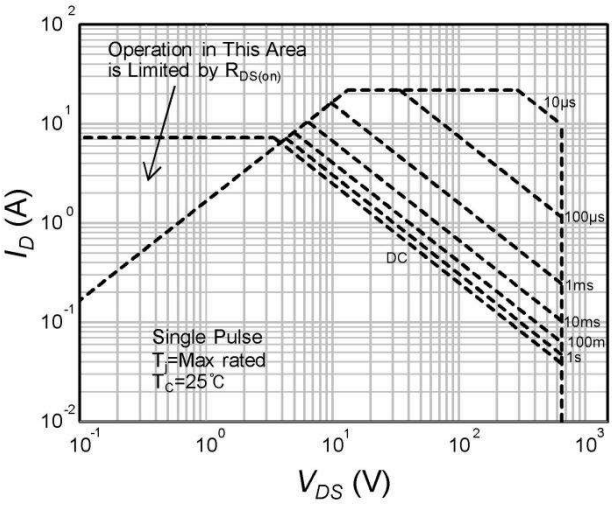


Fig.14 Maximum Safe Operating Area



■ Test Circuit

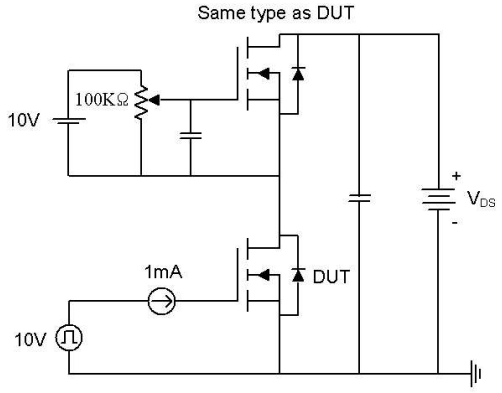


Fig15-1. Gate charge measurement circuit

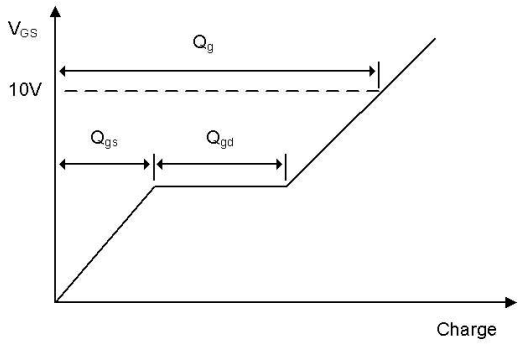


Fig15-2. Gate charge waveform

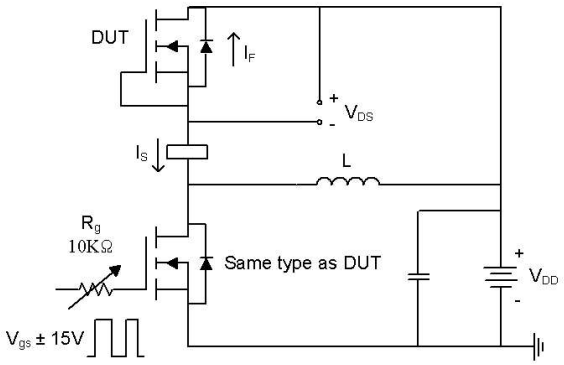


Fig16-1. Diode reverse recovery test circuit

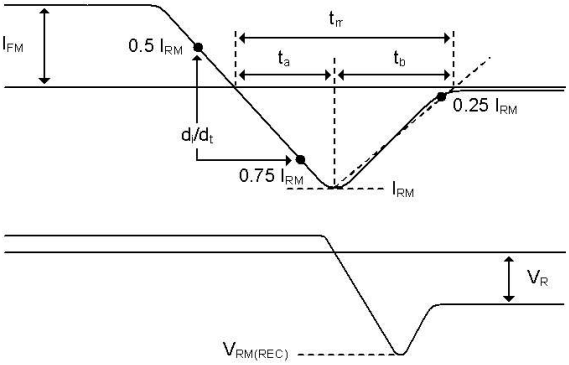


Fig16-2. Diode reverse recovery test waveform

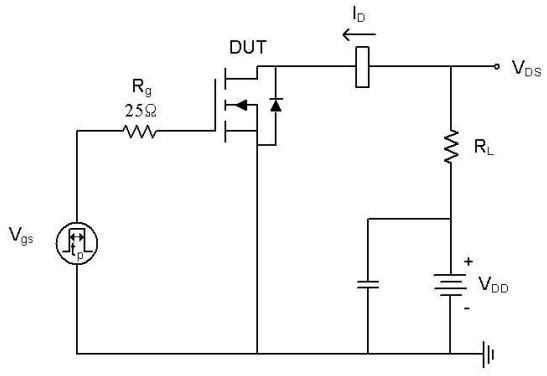


Fig17-1. Switching time test circuit for resistive load

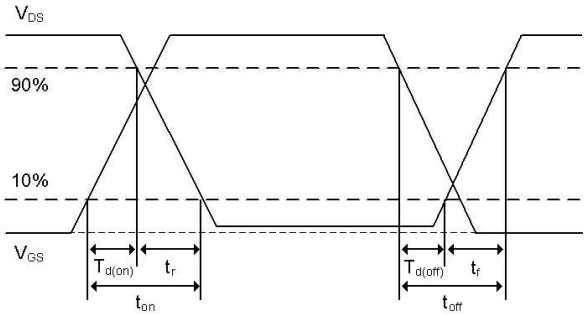


Fig17-2. Switching time waveform

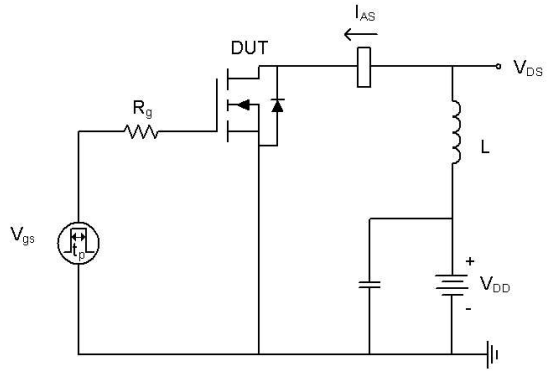


Fig18-1. Unclamped inductive load test circuit

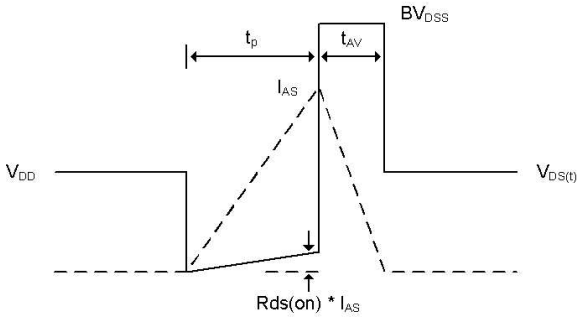
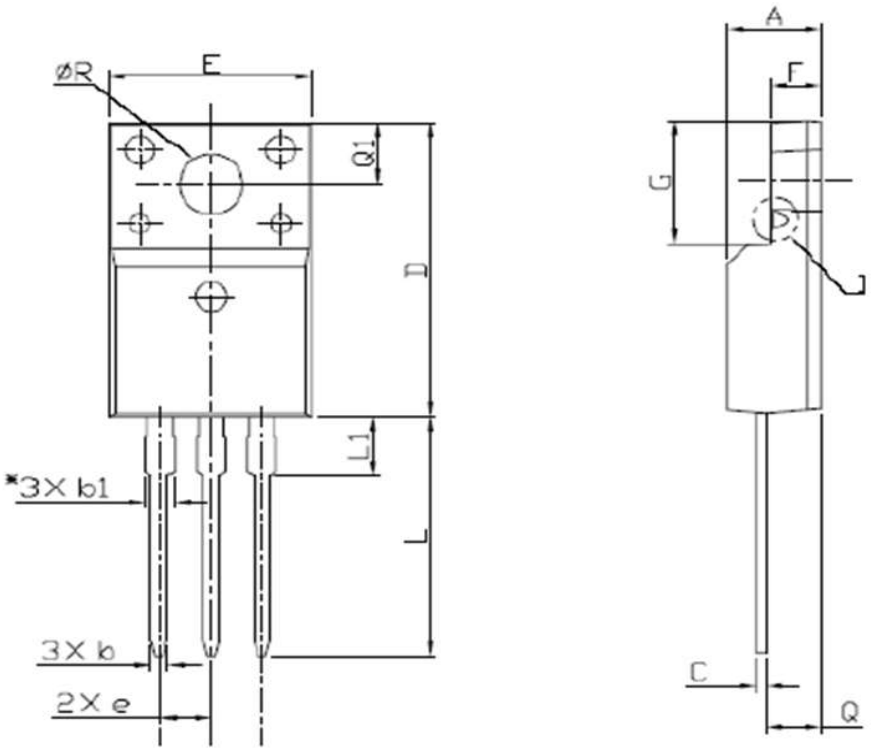


Fig18-2. Unclamped inductive waveform

■ Physical Dimension

3 Leads, TO-220F



Note : PKG Body Sizes exclude Mold Flash & Gate Burrs

[Unit:mm]

Symbol	Min	Nom	Max
A	4.50	-	4.93
b	0.63	-	0.91
b1	1.15	-	1.47
C	0.33	-	0.63
D	15.47	-	16.13
E	9.60	-	10.71
e	-	2.54	-
F	2.34	-	2.84
G	6.48	-	6.90
L	12.50	-	13.72
L1	2.79	-	3.67
Q	2.52	-	2.96
Q1	3.10	-	3.50
ØR	3.00	-	3.55